



Attorney Docket No.: 0553-0401

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Yoshifumi TANADA)
Serial No.: 10/807,692)
Filed: March 24, 2004)
For: Circuit For Inspecting Semiconductor)
Device And Inspecting Method)
Examiner: Vibol Tan)
Art Unit: 2819)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
the Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450 on

February 15 2006

(Date of Deposit)

Shannon Wallace

Name of applicant, assignee, or Registered Rep.

Shannon Wallace 2/15/06

Signature

Date

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT D (AFTER FINAL)

In response to Final Rejection of November 7, 2005, a RCE and one month extension of time being submitted herewith, please amend the above-identified application as follows: